Realistic TRC-481 Service Manual (21-1550)

REALISTIC®

Service Manual

21-1550

TRC-481
40-CHANNEL
CLASS D C.B. MOBILE
TRANSCEIVER
Catalog Number: 21-1550

CONTENTS

SPECIFICATIONS

General

Transmitter ---------- Crystal controlled PLL synthesizer, amplitude modulation
Receiver ---------- Crystal controlled double conversion, superheterodyne system
Communication frequencies ---------- All 40 CB channels (26.965 to 27.405 MHz)
Voltage operation ---------- 12 – 16V DC (negative ground vehicles)
Temperature and humidity range ---------- –22° F to +140° F (–30° C to +60° C) and 10% to 90%
Transmitter/Receiver switching ---------- Electrical

Standard Test Conditions

Power supply voltage ---------- 13.8V DC
Modulation frequency and modulation percentage ---------- 1000Hz, 30%
Receiver output power ---------- 500mW at external SP
Receiver output load impedance ---------- 8 ohms, non-inductive, resistive
Antenna load impedance of transmitter/receiver ---------- 50 ohms, non-inductive, resistive
Measuring channel ---------- 18
Ambient conditions
Temperature ---------- 77° F (25° C)
Humidity ---------- 40 to 70% RH

Transmitter		**Unit**	**Nominal**	**Limit**
Frequency tolerance at 77° F (25° C) (5 minutes after switch on)		Hz	± 100	± 1300
Carrier power at no modulation		W	3.9	3.6 – 4.4
Modulation attack time		m sec.	18	25
Modulation release time		m sec.	300	300 ± 200
Modulation distortion at 1 kHz 80% modulation		%	3	6
Spurious emission 2nd/3rd/4th/5th/6th 7th/8th/9th/10th		dB	– 70	– 60
Modulation 100% capability positive/negative		%	90	80
Current drain at no modulation		mA	1100	1300
at 80% modulation		mA	1500	2000
Modulation frequency response (1 kHz 0dB reference)				
450 Hz, EIA		dB	– 6	– 6 ± 3
2.5 kHz, EIA		dB	– 6	– 6 ± 3
Carrier power uniformity CH to CH at no modulation		W	0.2	0.5
Microphone sensitivity for AM 50% modulation		mV	1.0	2.0
AMC range between 50 to 100% modulation		dB	40	30
Occupied band width	± 5.0 kHz	dB	– 35	– 26
	± 7.5 kHz	dB	– 35	– 26
	± 10.0 kHz	dB	– 45	– 35
	± 12.5 kHz	dB	– 45	– 35
	± 15.0 kHz	dB	– 45	– 35
	± 17.5 kHz	dB	– 45	– 35
	± 20.0 kHz	dB	– 65	– 60
	± 22.5 kHz	dB	– 65	– 60

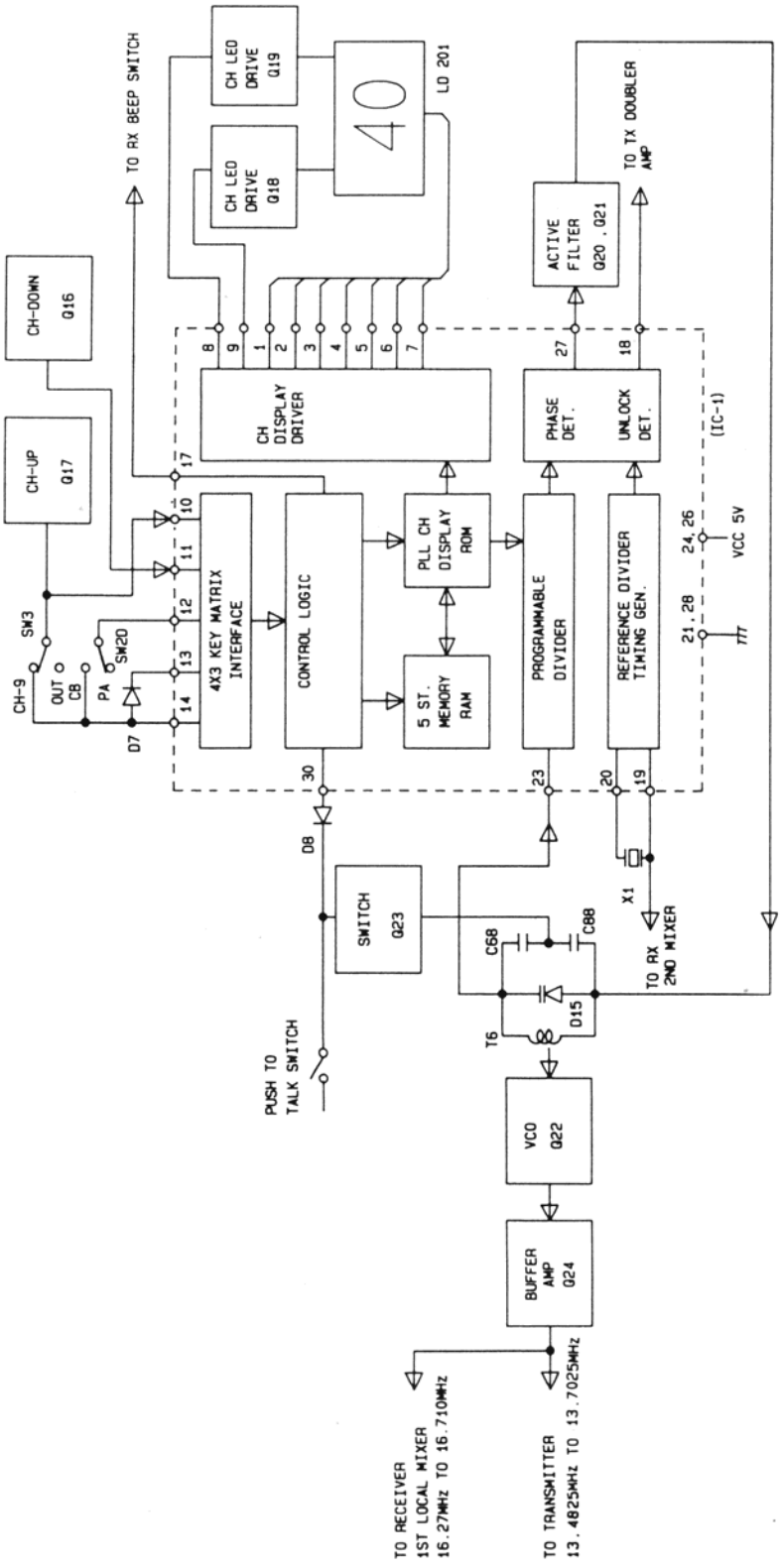
Receiver	**Unit**	**Nominal**	**Limit**
Maximum sensitivity	μV	0.3	0.6
Sensitivity for S/N 10 dB	μV	0.5	1.0
Squelch sensitivity at threshold	μV	0.7	1.4
at tight	μV	1000	355 – 2820
AGC figure of merit for – 10 dB audio output (Reference RF input 50 mV)	dB	90	70
Overload AGC characteristics from 50 mV to 1V	dB	3	3 ± 6
Overall audio fidelity (1 kHz 0 dB reference)			
lower frequency 450 Hz	dB	– 6	– 6 + 3
upper frequency 2500 Hz	dB	– 6	– 6 + 3
Adjacent channel selectivity (10 kHz)	dB	60	55
Maximum audio output power	W	6.0	4.5
Audio output power at 10% THD	W	5.0	3.5
THD at 500 mW AM: 1 mV input			
30% modulation	%	2.5	5
50% modulation	%	3	6
80% modulation	%	4	8
S/N ratio at 1 mV input	dB	40	35
Image rejection ratio (1st IF/2nd IF)	dB	45	35
1/2 IF rejection ratio (2nd IF)	dB	60	50
IF rejection ratio (1st IF/2nd IF)	dB	70	60
Spurious rejection ratio	dB	50	40
Skirt rejection, 20 kHz single signal	dB	60	50
Cross modulation, RS standard	dB	50	40
Desensitivity at 100 μV desired, 20 kHz away, 3 dB desensitivity	dB	50	40
Oscillator on voltage	V	8.0	10
Current drain at no signal	mA	200	300
Current drain at maximum output	mA	1000	1500
Local emission (Antenna Terminal)	dB m	– 73	– 67

Public Address	**Unit**	**Nominal**	**Limit**
Maximum output power	W	6.0	4.5
10% THD output power	W	5.0	3.5
Microphone sensitivity for PA 4W output at 1 kHz	mV	3	10
Frequency response			
upper frequency 2500 Hz	dB	– 6	– 6 ± 3
lower frequency 450 Hz	dB	– 6	– 6 ± 3
Current drain at maximum power	mA	1200	1500

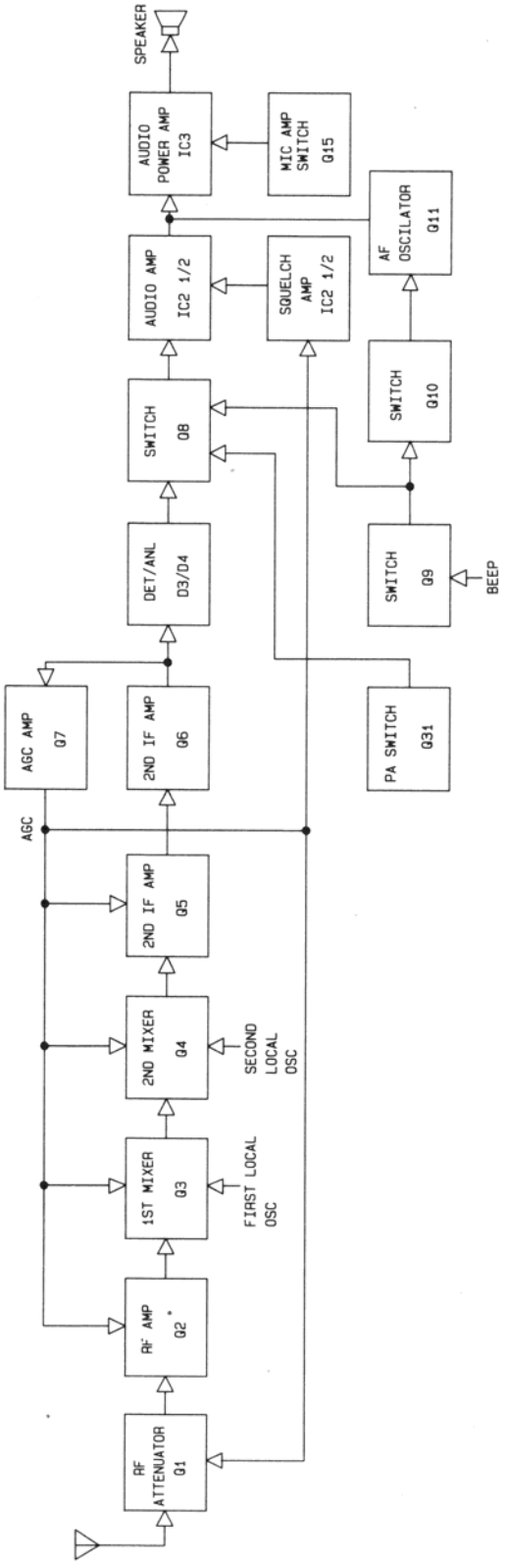
Note: Nominal specs represent the design specs. All units should be able to approximate these — some will exceed and some might drop slightly below these specs. Limit specs represent the absolute worst condition that still might be considered acceptable; in no case should a unit fail to meet limit specs.

BLOCK DIAGRAMS

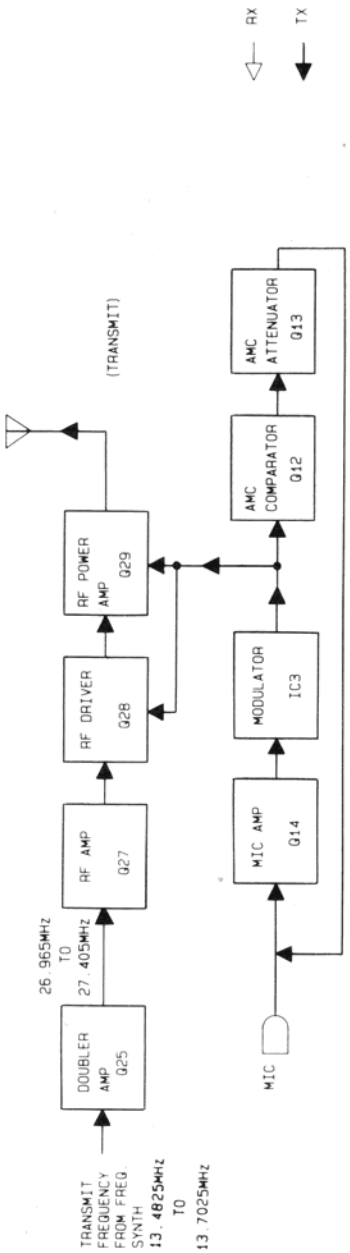
Frequency Synthesizer



Receive



Transmit



CIRCUIT DESCRIPTION

General

The TRC-481 is a 40-channel, crystal controlled mobile transceiver which consists of a PLL-synthesizer circuit, a receiver circuit and a transmitter circuit. Diode D14 is a polarity-protector. Power is supplied by a car battery (13.8 VDC). Refer to the Block Diagram and the Schematic Diagram as you read the following descriptions.

PLL Synthesizer Section

The TRC-481 uses a Phase-Locked-Loop (PLL) circuit to synthesize the local-oscillator frequencies for receiving and transmitting. It employs one IC and only one crystal. IC1 is a CMOS large scale integrated circuit containing a reference oscillator, phase detector, active low pass filter, reference divider (1/4096 for transmit and receive) and a programmable divider.

The programmable divider directly divides the output of the VCO (voltage controlled oscillator) down to a 2.5 kHz signal. Crystal X1 provides a reliable frequency standard which controls the local-oscillator frequencies. The reference-frequency divider inside IC1 counts down the oscillator signal to 1/4096, and passes it on to the phase detector, where it is compared with the 2.5 kHz signal from the programmable divider. An error voltage is generated by the phase detector, which is proportional to the phase difference between the two 2.5 kHz signals.

This error voltage appears at collector of Q20, Q21 and passes through the active LPF (low pass filter), where the error voltage is integrated and harmonics and noise are filtered out. The resulting DC voltage is applied to the varicap diode D15. Its capacity varies with the applied DC voltage. Because of this capacity change, the output frequency of the VCO is corrected. With proper circuit design and precise adjustments, the VCO frequency is accurate and precise when the system is "locked".

This means that the phase detector senses no phase differences between the two 2.5 kHz signals, and the VCO generates a frequency that is as accurate and stable as the reference crystal oscillator. The VCO circuit consists of D15, Q22 and T6.

The circuit is connected in the form of a hartley oscillator with varicap diode D15 as part of the tank circuit. The VCO circuit generates a signal ranging from 13.4825 to 16.710 MHz. The IC1 also includes an unlock-signal-detector circuit. Should the condition occur, the output at pin 18 of IC1, which is normally open, will be shorted to ground. This means that VCO frequency (1/2 carrier for transmitting) is "sunk" to pin 18 of IC1 and the transmitter circuits are inhibited.

Transmitter Circuit

RF Amplication

The output of doubler amp Q25 is fed through doubler tuning (27 MHz) T7 and T8 to the base of buffer amp Q27. The output is then supplied through tuning circuit T9 to RF driver amp Q28. The Q28 output capacitance is divided by tuning circuit L7, C103 and passed through tuning circuit L8 and C104 to the base of final RF stage Q29. The Q29 output is supplied to the antenna through L-C turning circuit.

Suppression of Spurious Radiation

The tuning circuit between frequency synthesizer and final amp Q29 and 3-stage "PI" network C107, L11, C108, C2, L13 and C1 in the Q29 output circuit serve to suppress spurious radiation. This network serves to impedance match Q29 to the antenna and to reduce spurious content to acceptable levels. In-band spurious is reduced to acceptable levels by filtering.

Limiting Power

During factory alignment, the series base resistor of final Q29 (R114) is selected to limit the available power to slightly more than 4 watts. The tuning is adjusted so the actual power is from 3.6 to 3.9 watts, and there are no other controls for adjusting power.

Modulation

The mic input is fed to mic amp Q14 and then to audio power IC3, which feeds the signal to the modulation transformer T5. The audio output at the set-up transformer of T5 is fed in series with the B+ voltage through diode D13 to the collectors of Q28 and final Q29 to collector modulate both these stages.

Limiting Modulation

A portion of the modulating voltage is fed through base of Q12 which turns on Q13 which attenuates the mic input to mic amp Q14. The resulting feedback loop keeps the modulation from exceeding 100 percent for inputs approximately 40 dB greater than that required to produce 50 precent modulation. The attack time is about 18 milli seconds, and the release time is about 350 milli seconds.

Receiver Circuit

Receiver

The receiver is a double conversion superheterodyne with first IF at 10.695 MHz and the second IF at 455 kHz. The synthesizer supplies the first local oscillator 10.695 MHz below the received frequency and the second local oscillator at 10.240 MHz.

The detector output provides reverse AGC to all previous stages except Q6. The detect and AGC voltage is also amplified by Q7, used to feed RF attenuator Q1, and squelch amp IC2 (2/2). The channel key-in tone circuit is Q9, Q10, Q11, Q8, and Q31.

Indicators

Channel Indication

Indicates the selected channel by 2-digit segment LEDs. The LEDs light dynamically by the outputs from IC1.

The output from pin 8 (D1) of IC1 controls the lighting of the 1st digit through Q19, and the output from pin 9 (D2) of IC1 controls the lighting of the 2nd digit through Q18.

The output ports of IC1; from pin 1 (SA) to pin 7 (SG), control the lighting of each segment of each digit.

TX / RX Indication

TX Mode Indication:
When the PTT switch is pressed, Q26 turns on and LD203 lights.

RX Mode Indication:
When the unit is in the receiver mode by turning-on of the power switch (VR1-SW), Q32 turns on and LD202 lights.

CH9 / PA Indication

When the CH9 / OUT switch on the front panel is set to CH9, LD201 flashes and displays "9."

When the PA / CB switch is set to PA, LD201 displays "PA."

FREQUENCIES GENERATED AND MIXED TO OBTAIN EACH CHANNEL

CHANNEL	FREQUENCY (MHz)	RX ($\overline{TX}$ = 1)		TX ($\overline{TX}$ = 0)	
		N	FVCO	N	FVCO
1	26.965	6508	16.27	5393	13.4825
2	26.975	6512	16.28	5395	13.4875
3	26.985	6516	16.29	5397	13.4925
4	27.005	6524	16.31	5401	13.5025
5	27.015	6528	16.32	5403	13.5075
6	27.025	6532	16.33	5405	13.5125
7	27.035	6536	16.34	5407	13.5175
8	27.055	6544	16.36	5411	13.5275
9	27.065	6548	16.37	5413	13.5325
10	27.075	6552	16.38	5415	13.5375
11	27.085	6556	16.39	5417	13.5425
12	27.105	6564	16.41	5421	13.5525
13	27.115	6568	16.42	5423	13.5575
14	27.125	6572	16.43	5425	13.5625
15	27.135	6576	16.44	5427	13.5675
16	27.155	6584	16.46	5431	13.5775
17	27.165	6588	16.47	5433	13.5825
18	27.175	6592	16.48	5435	13.5875
19	27.185	6596	16.49	5437	13.5925
20	27.205	6604	16.51	5441	13.6025
21	27.215	6608	16.52	5443	13.6075
22	27.225	6612	16.53	5445	13.6125
23	27.255	6624	16.56	5451	13.6275
24	27.235	6616	16.54	5447	13.6175
25	27.245	6620	16.55	5449	13.6225
26	27.265	6628	16.57	5453	13.6325
27	27.275	6632	16.58	5455	13.6375
28	27.285	6636	16.59	5457	13.6425
29	27.295	6640	16.60	5459	13.6475
30	27.305	6644	16.61	5461	13.6525
31	27.315	6648	16.62	5463	13.6575
32	27.325	6652	16.63	5465	13.6625
33	27.335	6656	16.64	5467	13.6675
34	27.345	6660	16.65	5469	13.6725
35	27.355	6664	16.66	5471	13.6775
36	27.365	6668	16.67	5473	13.6825
37	27.375	6672	16.68	5475	13.6875
38	27.385	6676	16.69	5477	13.6925
39	27.395	6680	16.70	5479	13.6975
40	27.405	6684	16.71	5481	13.7025

VCO (TX) = FREQUENCY ÷ 2
VCO (RX) = FREQUENCY – 10.695MHz (IF)
CH 1: VCO (TX) = 26.965 ÷ 2 = 13.4825
VCO (RX) = 26.965 – 10.695 = 16.27

ALIGNMENT

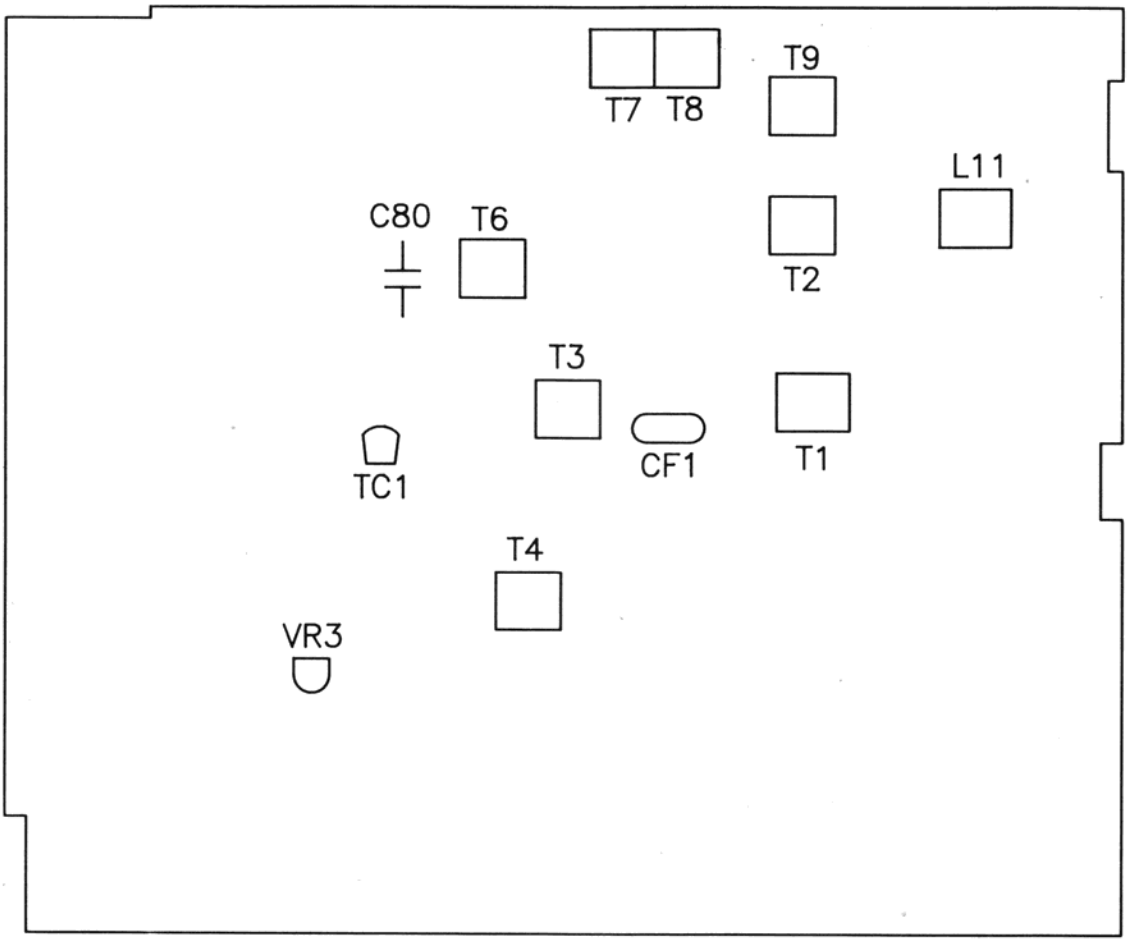


Figure 1

PLL SECTION

Test Equipment Required

- Frequency counter
- DC voltmeter (about 100k ohm)
- DC power supply (13.8V, 3 Amp)

Note: Figure 1 provides test point and all alignment location information.

Test Set-up

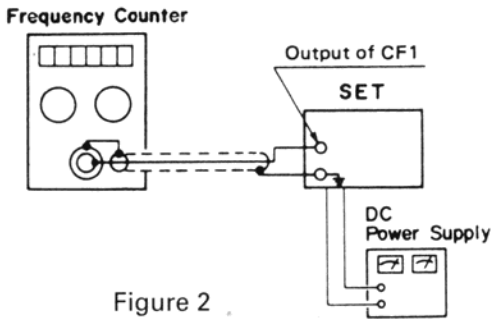


Figure 2

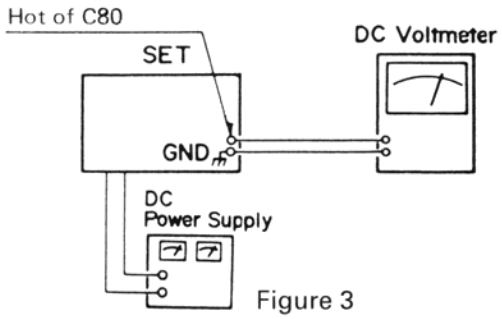


Figure 3

Alignment Procedure

STEP	CONTROL SETTING	OUTPUT INDICATOR CONNECTION	ADJUST	ADJUST FOR
1	Alignment of Ref. Osc.			
	MIC: Receive POWER: On VOLUME: Optional SQUELCH: Optional Channel Selector: Channel 19	Connect frequency counter to output of CF1. (Figure 2)	TC1	Adjust for 10.240MHz ±100Hz indication on frequency counter.
2	Alignment of VCO			
	MIC: Transmit POWER: On VOLUME: Optional SQUELCH: Optional Channel Selector: Channel 40	Connect DC voltmeter to hot of C80. (Figure 3)	T6	Adjust for 5.0V indication on DC voltmeter.
3	MIC: Receive POWER: On VOLUME: Optional SQUELCH: Optional Channel Selector: Channel 1	Same as Step 2.	Check the indication on DC voltmeter (must be 2.5–3.5V). If DC voltmeter does not indicate 2.5–3.5V, readjust T6 and return to step 2.	

TRANSMITTER SECTION

Test Equipment Required

- RF power meter
- 50 ohm load (non-inductive)
- DC power supply
  (13.8V, 3 Amp)
- Field strength meter
  (or spectrum analyzer with RF attenuator)
- Frequency counter
- Coupler

Note: Figure 1 provides test point and all alignment location information.

Test Set-up

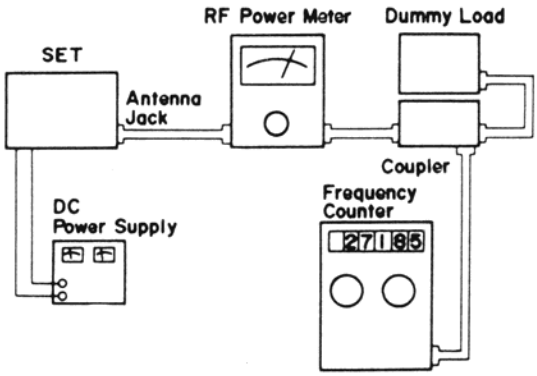


Figure 5

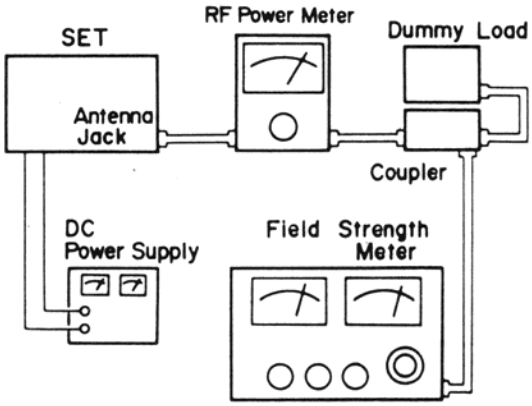


Figure 6

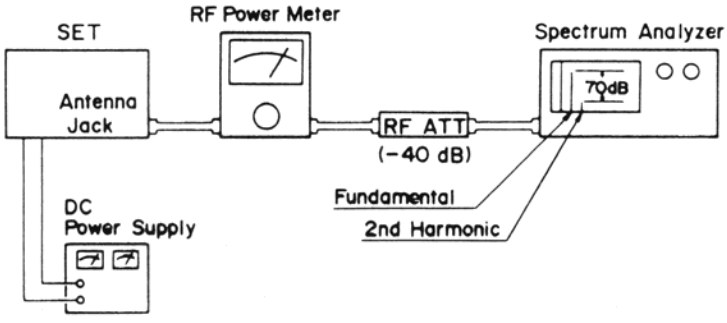


Figure 7

Alignment Procedure

STEP	CONTROL SETTING	OUTPUT INDICATOR CONNECTION	ADJUST	ADJUST FOR
1	Alignment of Overall			
	Set channel selector to CH19.	Connect dummy load and frequency counter through coupler to RF power meter. Connect RF power meter to ANT jack on set. (Figure 5)	T7, T8 T9, L11	Adjust for maximum indication on RF power meter.
2	Repeat Step 1 twice or 3 times.			
3	Realignment of T9			
	Set channel selector to CH1.	Same as Step 1.	T9	Adjust for maximum indication on RF power meter.
4	Set channel selector from CH1 to CH19, then from CH19 to CH40.	Same as Step 1.	Check that difference in RF output power between channels is less than 0.2W.	
5	Same as Step 4.	Same as Step 1.	Check that RF output power is 3.8 to 4.2W on all channels with no modulation. If it is not within the above range, go back to steps 1 through 4 and readjust. If still improper, change R114 value.	
6	Alignment of Transmitter Frequency			
	Return to CH19.	Same as Step 1.	TC1	Make sure that the transmitter frequency is 27.185MHz ± 300Hz on frequency counter. If not, readjust TC1.
7	Set channel selector to CH1, CH19, and CH40.	Connect dummy load and field strength meter through coupler to RF power meter. Connect RF power meter to ANT jack on set. (Figure 6) Tune to 2nd harmonic frequency (54.37MHz) on field strength meter. Or connect spectrum analyzer, RF attenuator and RF power meter to ANT jack on set. (Figure 7)	Check level of fundamental and 2nd harmonic frequency (54.37MHz). Check suppression of 2nd harmonic frequency (54.37MHz) compared to fundamental (must be better than 60dB). Check all channels and if necessary, make sure that the 2nd harmonic frequency suppression is more than –63dB on all channels with no modulation. (Reference : –70dB)	

RECEIVER SECTION

Test Equipment Required

- RF signal generator
- Distortion meter
- SSVM
- Dummy load (8 ohm)
- DC power supply (13.8V, 3 Amp)

General Alignment Conditions

- Signal input must be kept as low as possible, to avoid overload and clipping. (Use highest possible sensitivity of output indicator.)
- Standard modulation is 1000Hz at 30% amplitude.
- A non-metalic alignment tool must be used for all adjustments.
- Power supply is adjusted for 13.8V DC, 3A.

Note: Figure 1 shows test point and all alignment location information.

Test Set-up

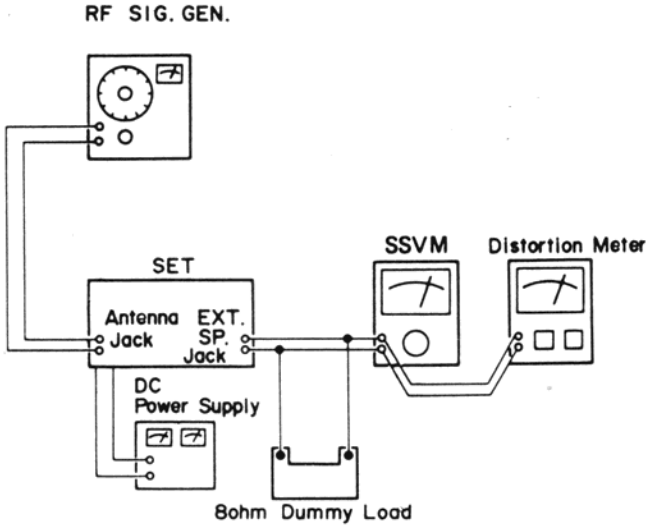


Figure 10

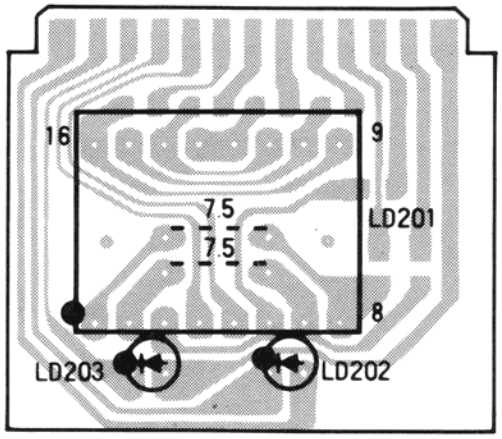
Alignment Procedure

STEP	SIGNAL SOURCE CONNECTION	OUTPUT INDICATOR CONNECTION	ADJUST	ADJUST FOR
1	Set channel selector to CH19.			
2	Turn VR1 (VOLUME) fully clockwise.			
3	Turn VR2 (SQUELCH) fully counterclockwise.			
4	Alignment of Overall			
	1) Set RF signal generator: 0.3μV at 1kHz, 30% mod. 2) Audio output is 500mW (Ref. output power).	1) Connect RF signal generator to ANT. jack. 2) Connect SSVM and distortion meter across EXT speaker jack with 8 ohm dummy load. (Figure 10)	T1, T2 T3, T4 L1	Adjust for maximum indication on SSVM.
5	Repeat Step 4 twice or three times.			
6	Realignment of T4			
	1) Set RF signal generator: 1mV at 1kHz, 80% mod. 2) Set VR1 so that audio output is 500mW.	Same as Step 4.	T4	Adjust for minimum indication on distortion meter.
7	Alignment of Squelch			
	Set RF signal generator 1 mV at 1 kHz, 30% mod. SQUELCH : FULLY clockwise.	Same as Step 4.		Adjust VR3 so that audio output is turned on.

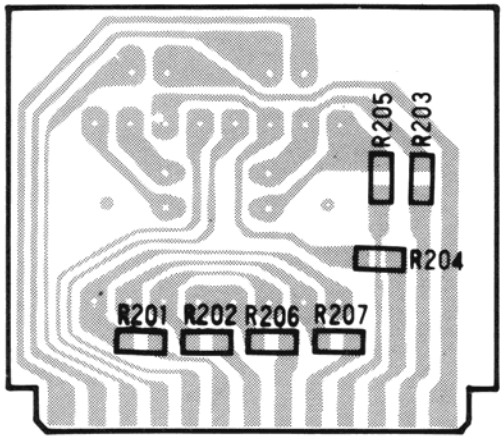
PCB TOP AND BOTTOM VIEW / WIRING DIAGRAM

DISPLAY PCB

Top View

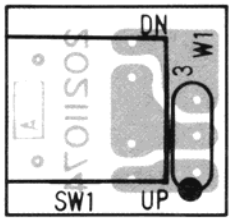


Bottom View

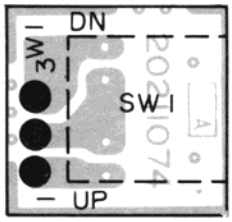


CHANNEL SWITCH PCB

Top View

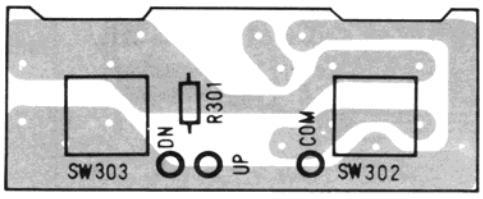


Bottom View

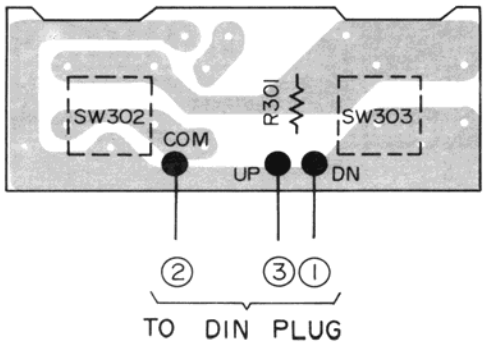


HAND MIC PCB

Top View

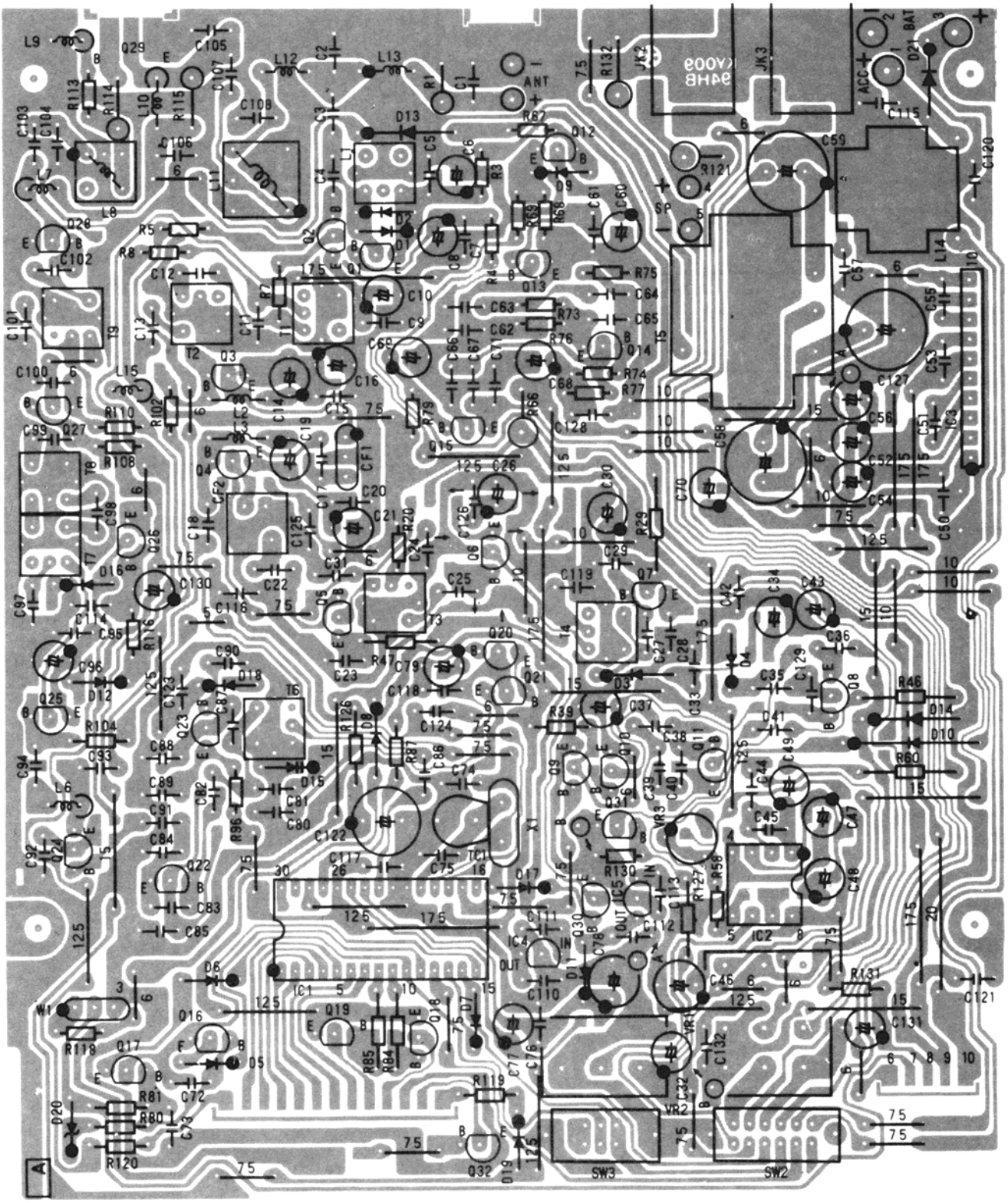


Bottom View



MAIN PCB

Top View



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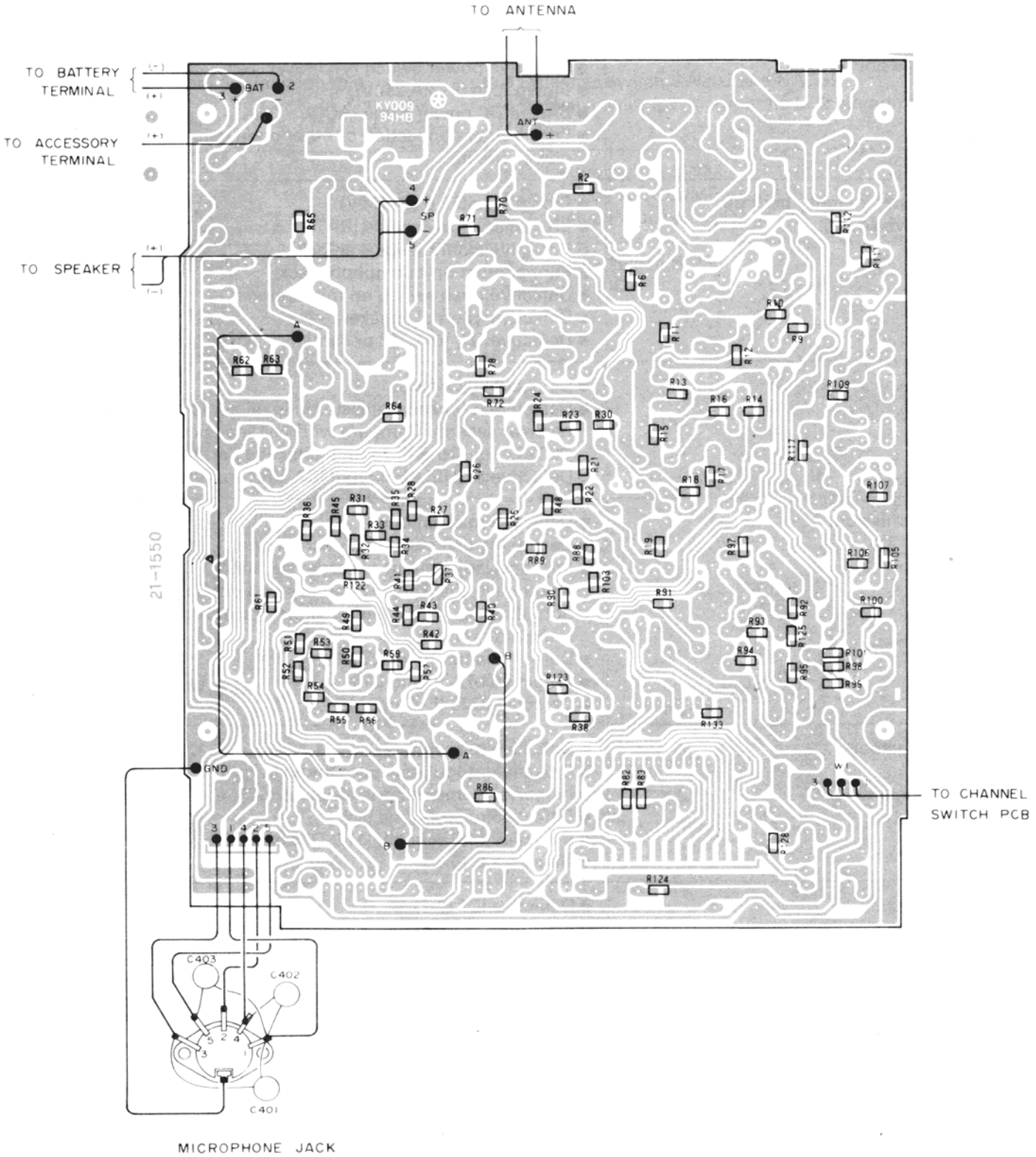
Bottom View


TO ANTENNA
TO BATTERY TERMINAL
TO ACCESSORY TERMINAL
TO SPEAKER
BAT
ANT
SP
KY009
94HB
21-1550
GND
TO CHANNEL SWITCH PCB
C403
C402
C401
MICROPHONE JACK