TC9106 PLL OPERATION ANALYSIS

1. Output Frequency of the Transmitter

Transmitting frequency, Ft is the output of the Transmitter Mixer IC2. One to the inputs of IC2 is the 1st Local frequency, Fvco , which is produced by the P.L.L. Local oscillator circuit, and the other is the transmitter local frequency of 10.240 MHz produced by TR 15. The sum of these frequencies make the transmitting frequency as follows.

$$FT = Fvco + 10.240\ Mhz$$

2. P.L.L. Local Oscillator

The output frequency of TR 11 is designated as Fvco and the output frequency of TR 15 is 10.240 MHZ. Both Fvco and 10.240 Mhz. are applied to IC 3. Fvco is divided by N at IC 3 and the divided frequency will be Fl:

$$\text{Therefore, } Fl = Fvco \div N$$

IC 3 also divides 10.24MHZ by 2048 and the divided frequency is designated as F2.

$$F2 = 10.24MHZ \div 2048 = 5Khz$$

Fl is compared with F2 at IC3 and if they are equal in frequencies, the phase locked loop is under the locked condition. Therefore, Fvco is determined by the following formula:

$$Fvco = N \times F2 = N \times 5KHz$$

Fvco is changeable at the increment of 10KHz by varying the program divide ratio, N. For example, the divide ratio, N is programmed to 3345 at the channel No. 1, the Fvco is calculated as follows:

$$Fvco = 3345 \times 5KHz = 16.725MHz$$

In the same manner, Fvco for channel No. 1 through No. 40 is determined as shown in Table A.

3. TRANSMITTER LOCAL OSCILLATOR

Transmitter local frequency of 10.240 MHz is produced by the oscillator, TR 15 and the output frequency is determined by the quartz crystal X 1.

4. CHANNEL SELECTION PROGRAM

The divide ratio of the programable frequency divider in IC 3 is determined through the code converter and transmit/receive mode switch in IC 3 by the voltage applied to the program input terminals, pin No. 10 through pin No. 17 of the IC 3.

The program input voltage for pin No. 10 through pin No. 17 are delivered from channel rotary switch according to channel number selected.

The Transmit/Receive mode switch in IC 3 changes the divide ratio of the programmable divider by changing the applied voltage at pin No. 8, low level for transmit and high level for receive.

Table A shows Frequency Chart of Fvco and Divide Ration vs. Antenna Frequency.

CIRCUIT DESCRIPTION

CIRCUIT FOR PREVENTION OF UNAUTHORIZED FREQUENCY EMISSION

This model is equipped with circuit which prevents transmission on unauthorized frequency at the time when the P.L.L. circuit is under unlocked condition or when the channel rotary switch is placed at the in-between channel.

When the P.L.L. circuit is not locked, or program data input is loaded which is outside of Channel 1 to 40, or channel rotary switch is switched from one channel to the next one, a program other than formulated is produced. However, even at the in-between channel, pin No. 4, in IC 3 produces low level digital control signal. This signal is delivered to the buffer amplifier, base of TR 9 and the transmitter mixer, pin No. 7 of IC 2. When this signal is in low level state, no output signal is produced from the transmitter mixer, IC 2, and TR 9. Thus the transmission of unauthorized frequency is prevented.

BLOCK DIAGRAM OF PLL

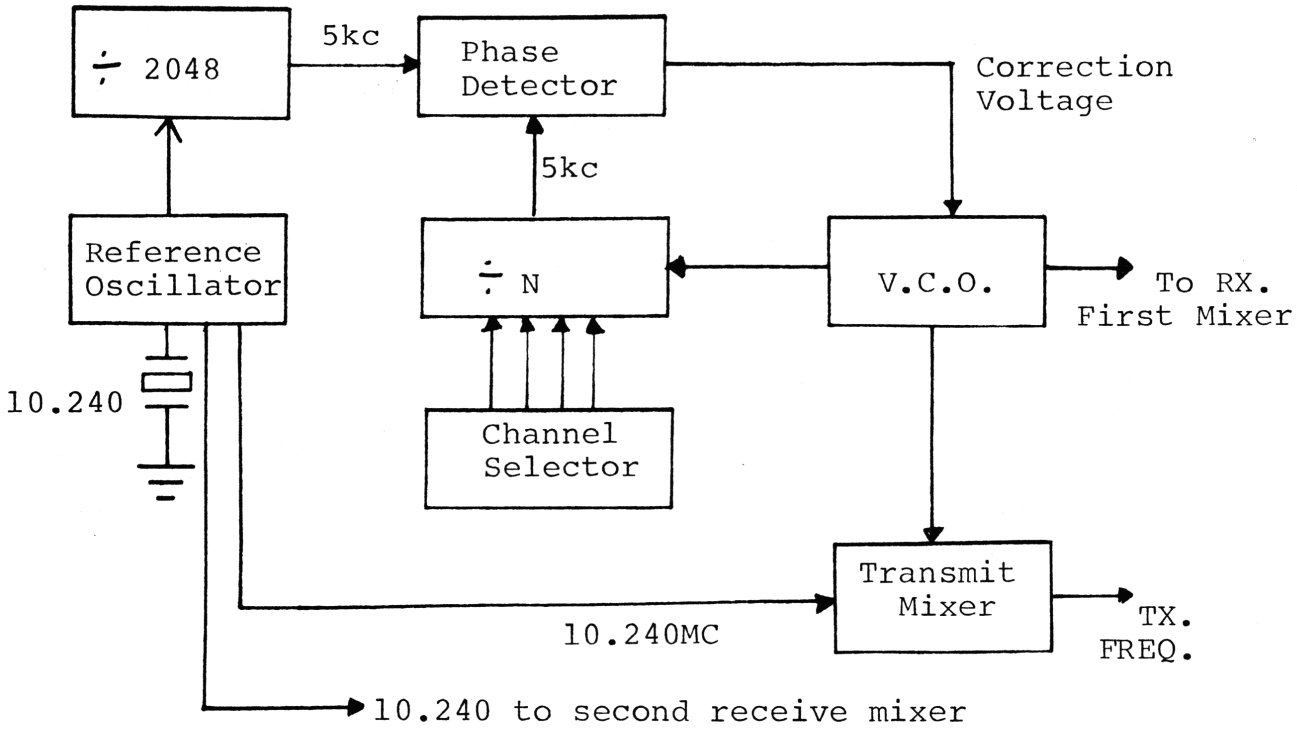

TABLE A FREQUENCY CHART OF FVCO AND DIVIDE RATIO N

Antenna Frequency (MHz)	Channel Number	For Transmit(R/T=H) Divide Ratio (N)	VCO Frequency (MHz)	For Receive(R/T=L) Divide Ratio (N)	VCO Frequency (MHz)
26.965	1	3,345	16,725	3,254	16,270
26.975	2	3,347	16,735	3,256	16,280
26.985	3	3,349	16,745	3,258	16,290
27.005	4	3,353	16,765	3,262	16,310
27.015	5	3,355	16,775	3,264	16,320
27.025	6	3,357	16,785	3,266	16,330
27.035	7	3,359	16,795	3,268	16,340
27.055	8	3,363	16,815	3,272	16,360
27.065	9	3,365	16,825	3,274	16,370
27.075	10	3,367	16,835	3,276	16,380
27.085	11	3,369	16,845	3,278	16,390
27.105	12	3,373	16,865	3,282	16,410
27.115	13	3,375	16,875	3,284	16,420
27.125	14	3,377	16,885	3,286	16,430
27.135	15	3,379	16,895	3,288	16,440
27.155	16	3,383	16,915	3,292	16,460
27.165	17	3,385	16,925	3,294	16,470
27.175	18	3,387	16,935	3,296	16,480
27.185	19	3,389	16,945	3,298	16,490
27.205	20	3,393	16,965	3,302	16,510
27.215	21	3,395	16,975	3,304	16,520
27.225	22	3,397	16,985	3,305	16,530
27.255	23	3,403	17,015	3,312	16,560
27.235	24	3,399	16,995	3,308	16,540
27.245	25	3,401	17,005	3,310	16,550
27.265	26	3,405	17,025	3,314	16,570
27.275	27	3,407	17,035	3,316	16,580
27.285	28	3,409	17,045	3,318	16,590
27.295	29	3,411	17,055	3,320	16,600
27.305	30	3,413	17,065	3,322	16,610
27.315	31	3,415	17,075	3,324	16,620
27.325	32	3,417	17,085	3,326	16,630
27.335	33	3,419	17,095	3,328	16,640
27.345	34	3,421	17,105	3,330	16,650
27.355	35	3,423	17,115	3,332	16,660
27.365	36	3,425	17,125	3,334	16,670
27.375	37	3,427	17,135	3,336	16,680
27.385	38	3,429	17,145	3,338	16,690
27.395	39	3,431	17,155	3,340	16,700
27.405	40	3,433	17,165	3,342	16,710

TABLE B TRUTH TABLE

Channel No.	Program Input Data							
Pin #	10	11	12	13	14	15	16	17
1	H	H	H	H	H	H	H	H
2	H	L	L	L	L	H	H	H
3	H	L	L	H	L	H	H	H
4	L	H	L	H	H	H	H	H
5	L	L	L	H	L	H	H	H
6	L	H	L	L	L	H	H	H
7	L	H	H	H	H	H	H	H
8	L	L	L	L	L	H	H	H
9	L	L	L	H	H	H	H	H
10	L	L	H	L	L	L	H	H
11	H	H	H	H	H	L	H	H
12	H	L	L	L	L	L	H	H
13	H	L	L	H	L	L	H	H
14	L	H	L	H	H	L	H	H
15	L	L	L	H	L	L	H	H
16	L	H	L	L	L	L	H	H
17	H	L	H	H	H	L	H	H
18	L	L	L	L	L	L	H	H
19	L	L	L	H	H	L	H	H
20	L	L	H	L	L	H	L	H
21	H	H	H	H	H	H	L	H
22	H	L	L	L	L	H	L	H
23	H	L	L	H	L	H	L	H
24	L	H	L	H	H	H	L	H
25	L	L	L	H	L	H	L	H
26	L	H	L	L	L	H	L	H
27	H	L	H	H	H	H	L	H
28	L	L	L	L	L	H	L	H
29	L	L	L	H	H	H	L	H
30	L	L	H	L	L	L	L	H
31	H	H	H	H	H	L	L	H
32	H	L	L	L	L	L	L	H
33	H	L	L	H	L	L	L	H
34	L	H	L	H	H	L	L	H
35	L	L	L	H	L	L	L	H
36	L	H	L	L	L	L	L	H
37	H	L	H	H	H	L	L	H
38	L	L	L	L	L	L	L	H
39	L	L	L	H	H	L	L	H
40	L	L	H	L	L	L	H	L

H: High level (more than 6.0 Volts D.C.)
L: Low level (less than 2.0 Volts D.C.)