REALISTIC TRC 209 (GRE 7189 PLL-VCO)

The following is a description of how the PLL System in this set Functions.

The PLL Circuit consists of a Phase Detector, Low Pass Filter and a Voltage Controlled Oscillator which uses a Varicap Diode as the frequency control device. A 10.240 rock is used as the reference frequency. This crystal is connected between Pins 9 and 10 of IC3. Pin 9 is the output for the 10.240 MHz and is processed by the PLL IC, as well as being used for the second mixer.

VCO Frequencies are divided by "N" as determined by the channel selector switch. Thus the resulting frequency is 2.5 KC. For channel 1, it will go like this; 16.270MHz ÷ 6508 = 2.5 KHz. Also, the reference oscillator frequency, 10.240MHz, is divided by 4096 resulting in another 2.5 KC frequency. These two 2.5KHz signals are fed to the Phase Detector. A DC Error Voltage is generated by the Phase Detector which is in proportion to the phase difference, plus effects of harmonics and noise. Pin 6 is the input to a Low Pass Filter, where the error voltage is integrated and harmonics and noises are filtered out. The resulting DC voltage is applied to the VCO varicap diode, whose capacity varies with applied DC voltage. When the Phase Detector senses no frequency or phase difference between the two 2.5 KHz signals, the system is Locked and the VCO generates a frequency which is as accurate and stable as the reference crystal oscillator. The channel selector switch provides a ROM code output which is connected to Pins 7-8, and 11-14; the IC converts these signals into binary code. The resulting code determines "N", the divisor which produces the required output frequency for each channel precisely spaced 10 KHz apart.

For transmit, the same VCO is used, which oscillates in the 13.5 MHz band. The actual transmit frequency is obtained by doubling this 13 MHz VCO frequency. These signals are divided by "N" as determined by the Channel Selector Switch. Thus, the circuits function in the same way, except for the divide by "N" number. This "N" number divisor change is controlled by Pin 5, the R/T Switch.

When the PLL is "Unlocked" an inhibit signal appears at the internal 6 BIT Counter and this signal is applied to the internal gate, turning it OFF. Thus, the Receiver and /or transmitter cannot operate in an unlocked condition.

TX:

Peak T5, T6, T7, L4, L7, L8.
VR9; Hi Power Adjust.
VR5; A.M.C.
VR6; RF Power Meter.