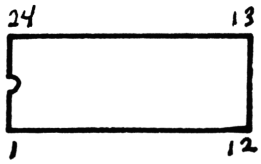
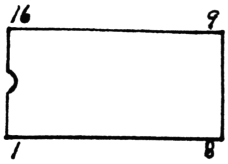
PLL PINOUT DIAGRAMS (CONT)

UPD 861C



Pin		
	1	Program Inputs P0
	2	P1
	3	P2
	4	P3
	5	P4
	6	P5
	7	P6
	8	P7
	9	5.12MHz
	10	Ref. Osc (10.240) input
	11	Ref. Osc. output
	12	Supply Voltage
	13	Input to programmable divider, greater than 3MHz
	14	Program input mode switch
	15	Output of prog. divider
	16	Phase detector input
	17	Output Ref divider-10Kc
	18	Phase det. input
	19	Output of active filter amp.
	20	Input of active filter amp.
	21	Error signal output of phase det.
	22	Loop locked - High level
	23	Ground
	24	Inhibit output normal - Low level

MN6040



Pin		
	1	+5 V
	2	Prog. Div. input
	3	Ref. divider input
	4	Ref divider input
	5	Ø det. output
	6	Lock det. output
	7	Program inputs P8 MSB
	8	P7
	9	P6
	10	P5
	11	P4
	12	P3
	13	P2
	14	P1
	15	P0
	16	Ground