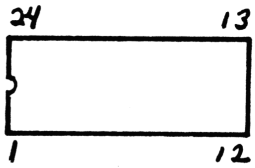
PLL PINOUT DIAGRAMS (CONT)

UPD 858C

Pin		
	1	Lock detector output. Normally low
	2	Output of Charge Pump-correct VCO
	3	Input low pass filter
	4	Output low pass filter
	5	Ref. Input to phase det./Charge Pump
	6	Output Ref. divider
	7	Ref. Freq. Select pin H÷1024; L÷2048
	8	5.12 MHz output
	9	Input Ref Osc.
	10	Output Ref Osc (10.240)
	11	Programmable divider input
	12	Supply voltage
	13	Program Input P0
	14	P1
	15	P2
	16	P3
	17	P4
	18	P5
	19	P6
	20	P7
	21	P8
	22	P9
	23	Ground
	24	10Kc Test Point



MM 55106

Pin		
	1	+5V
	2	Prog. Div. Input
	3	Ref. OSC. Inc. (10.240)
	4	Ref. OSC. Output
	5	5.12 MHz output
	6	Ref. Freq. Select
	7	Ø det. output to VCO
	8	Lock det. output
	9	Prog. Input MSB-P8
	10	P7
	11	P6
	12	P5
	13	P4
	14	P3
	15	P2
	16	P1
	17	LSB P0
	18	Ground