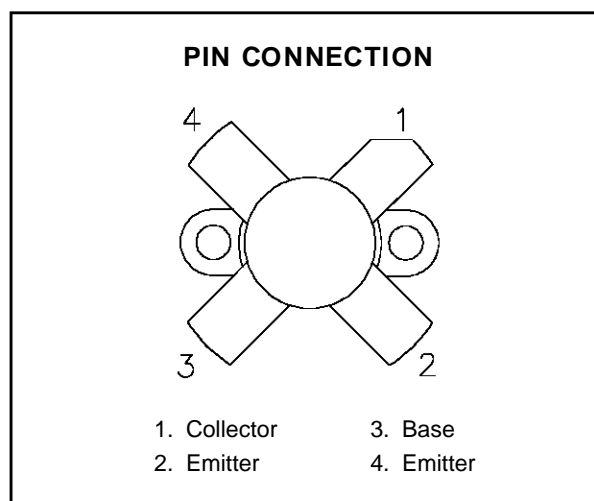
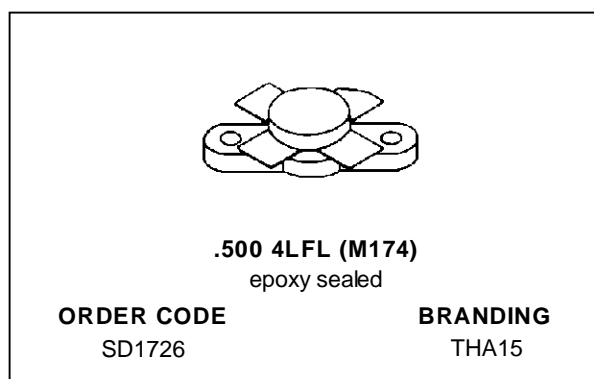


RF & MICROWAVE TRANSISTORS HF SSB APPLICATIONS

- OPTIMIZED FOR SSB
- 30 MHz
- 50 VOLTS
- IMD -30 dB
- COMMON EMITTER
- GOLD METALLIZATION
- P_{OUT} = 150 W PEP MIN. WITH 14 dB GAIN



DESCRIPTION

The SD1726 is a 50 V epitaxial silicon NPN planar transistor designed primarily for SSB communications. This device utilizes emitter ballasting to achieve extreme ruggedness under severe operating conditions.

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C)

Symbol	Parameter	Value	Unit
V _{CBO}	Collector-Base Voltage	110	V
V _{CEO}	Collector-Emitter Voltage	55	V
V _{EBO}	Emitter-Base Voltage	4.0	V
I _C	Device Current	10	A
P _{DISS}	Power Dissipation	233	W
T _J	Junction Temperature	+200	°C
T _{STG}	Storage Temperature	- 65 to +150	°C

THERMAL DATA

R _{TH(j-c)}	Junction-Case Thermal Resistance	0.75	°C/W
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SD1726 (THA15)

ELECTRICAL SPECIFICATIONS ($T_{case} = 25^{\circ}C$)

STATIC

Symbol	Test Conditions		Value			Unit
			Min.	Typ.	Max.	
BV_{CBO}	$I_C = 100mA$	$I_E = 0mA$	110	—	—	V
BV_{CES}	$I_C = 100mA$	$V_{BE} = 0V$	110	—	—	V
BV_{CEO}	$I_C = 100mA$	$I_B = 0mA$	55	—	—	V
BV_{EBO}	$I_E = 10mA$	$I_C = 0mA$	4.0	—	—	V
I_{CEO}	$V_{CE} = 30V$	$I_E = 0mA$	—	—	5	mA
I_{CES}	$V_{CE} = 60V$	$I_E = 0mA$	—	—	5	mA
h_{FE}	$V_{CE} = 6V$	$I_C = 1.4A$	18	—	43.5	—

DYNAMIC

Symbol	Test Conditions			Value			Unit
				Min.	Typ.	Max.	
P_{OUT}	$f = 30\text{ MHz}$	$V_{CE} = 50\text{ V}$	$I_{CQ} = 100mA$	150	—	—	W
G_P^*	$P_{OUT} = 150\text{ WPEP}$	$V_{CE} = 50\text{ V}$	$I_{CQ} = 100mA$	14	—	—	dB
IMD*	$P_{OUT} = 150\text{ WPEP}$	$V_{CE} = 50\text{ V}$	$I_{CQ} = 100mA$	—	—	-30	dBc
η_c^*	$P_{OUT} = 150\text{ WPEP}$	$V_{CE} = 50\text{ V}$	$I_{CQ} = 100mA$	37	—	—	%
C_{OB}	$f = 1\text{ MHz}$	$V_{CB} = 50\text{ V}$		—	—	220	pF

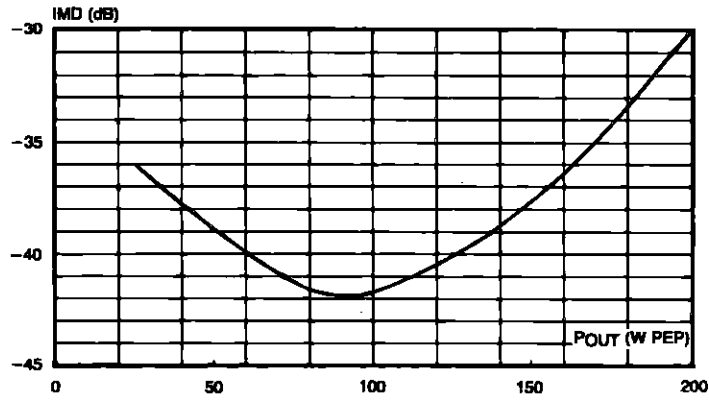
Note: The SD1726 is also usable in Class A at 40 V. Typical performance is:

$P_{OUT} = 30\text{ W PEP}$, $G_P = 14\text{ dB}$, $IMD = -40\text{ dBc}$

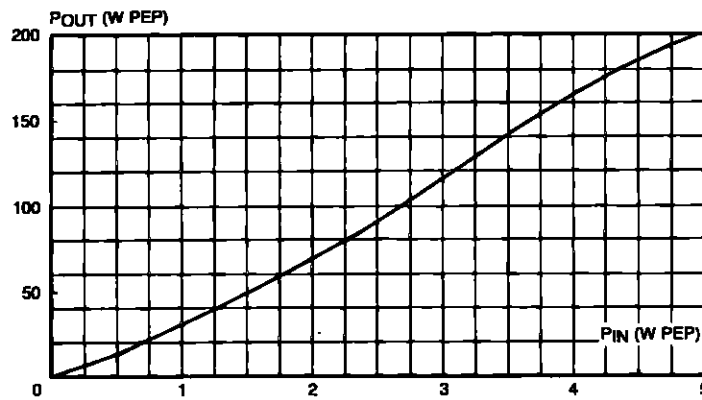
* $f_1 = 30.00\text{ MHz}$; $f_2 = 30.001\text{ MHz}$

TYPICAL PERFORMANCE

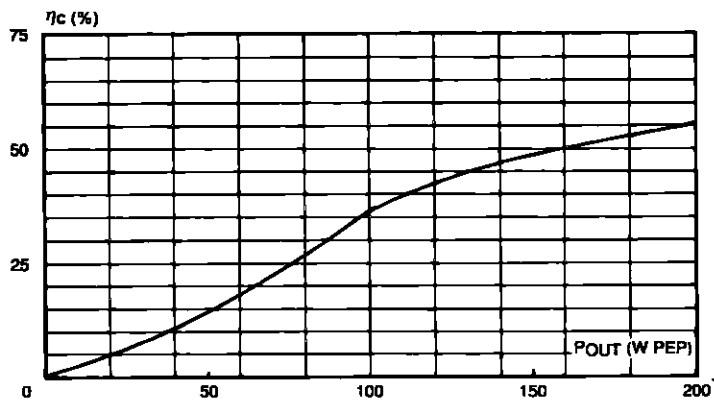
INTERMODULATION DISTORTION vs POWER OUTPUT PEP



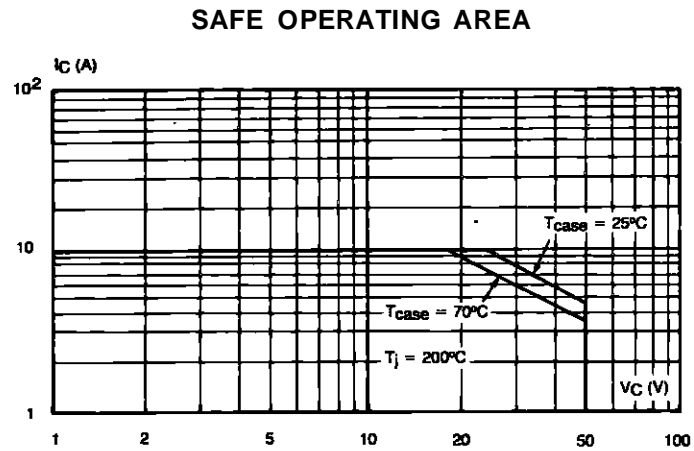
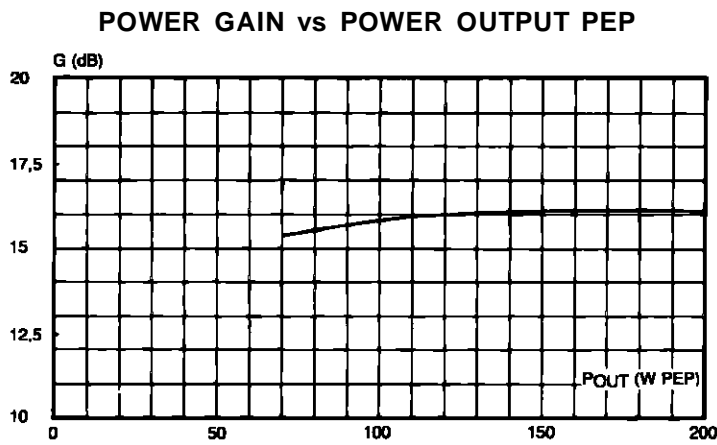
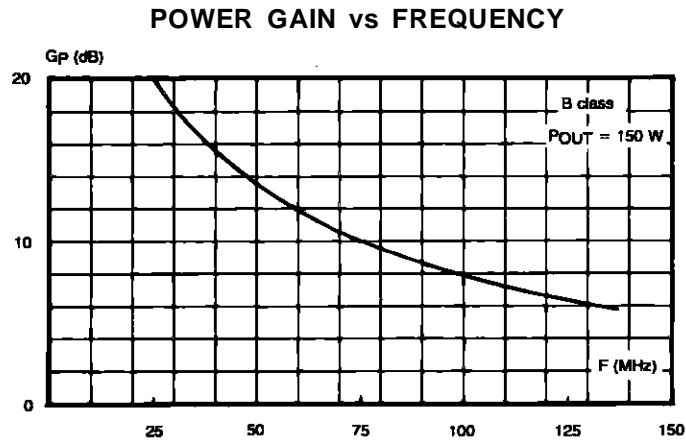
POWER OUTPUT PEP vs POWER INPUT



COLLECTOR EFFICIENCY vs POWER OUTPUT PEP

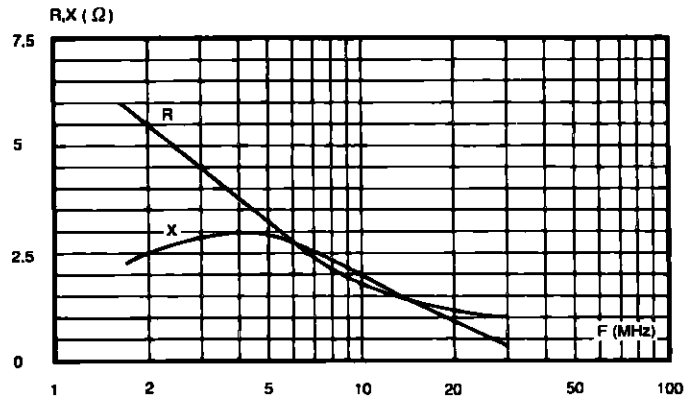


TYPICAL PERFORMANCE (cont'd)

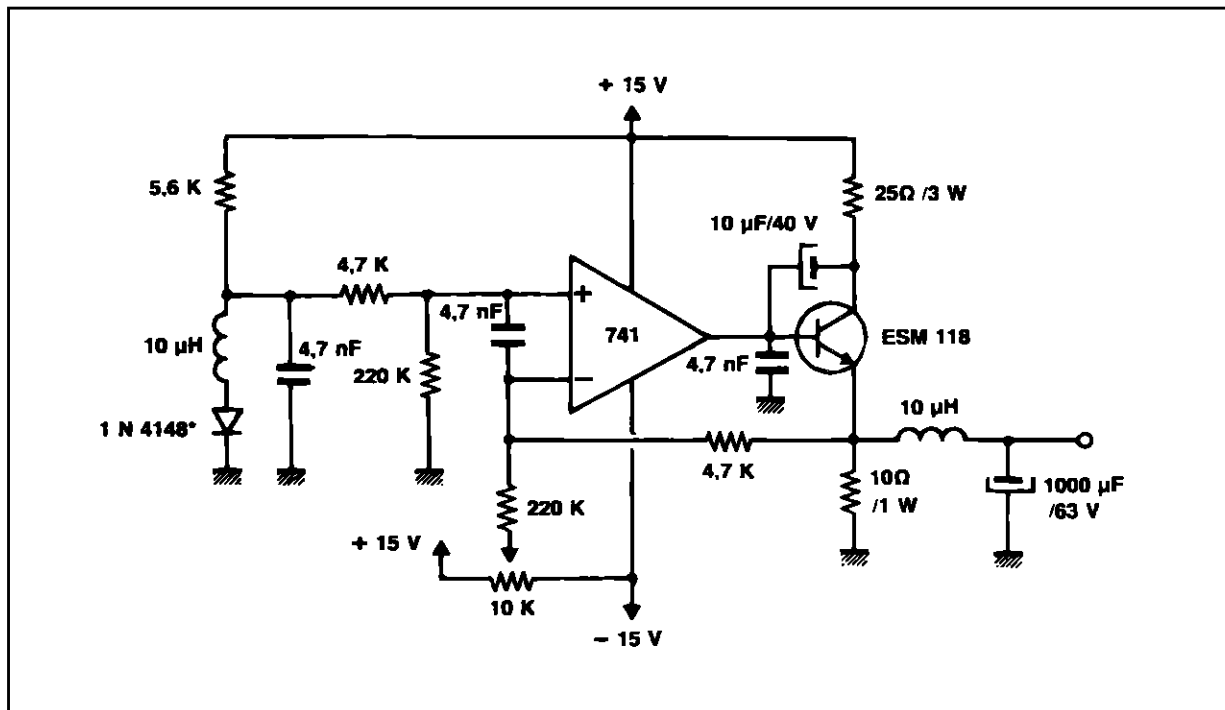


IMPEDANCE DATA

TYPICAL INPUT IMPEDANCE

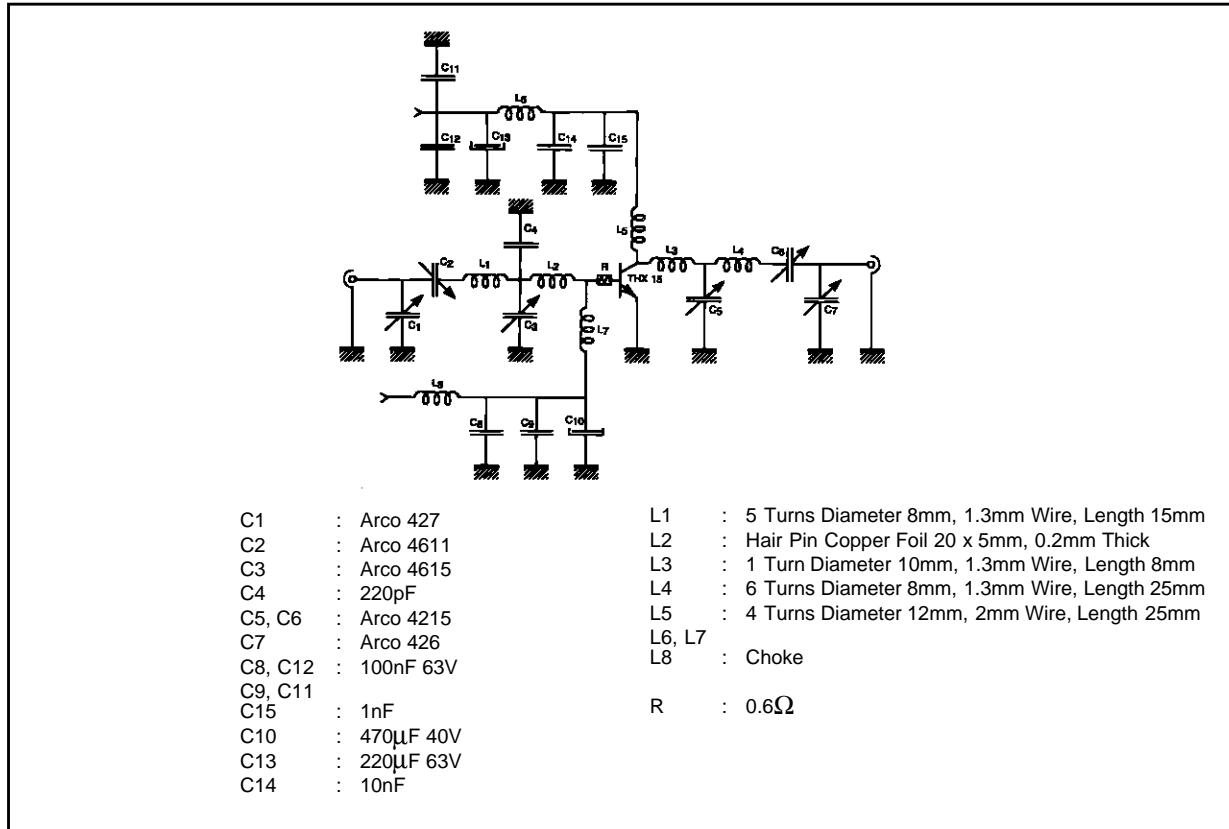


BIAS CIRCUIT

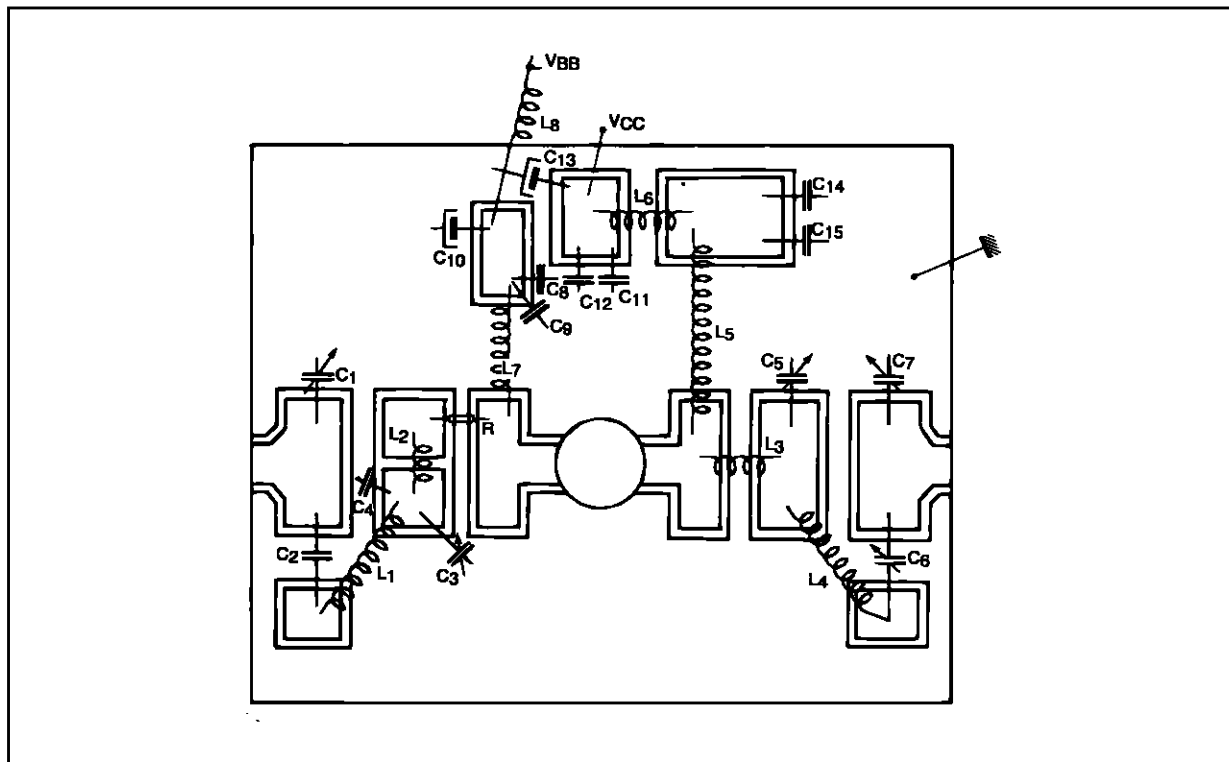


SD1726 (THA15)

TEST CIRCUIT - CLASS AB - 30 MHz

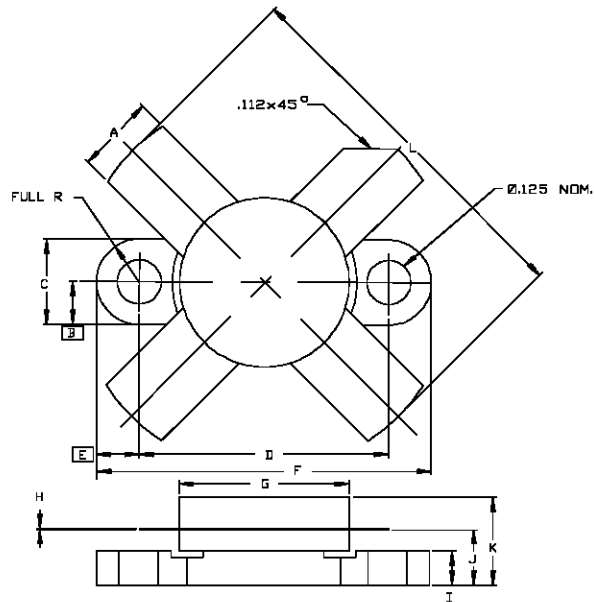


MOUNTING CIRCUIT - CLASS AB - 30MHz



PACKAGE MECHANICAL DATA

Ref.: Dwg. No.12-0174



SGS-THOMSON MICROELECTRONICS			CONT'D		
	MINIMUM Inches/mm	MAXIMUM Inches/mm		MINIMUM Inches/mm	MAXIMUM Inches/mm
A	.220/5,59	.230/5,84	K		.280/7,11
B	.125/3,18		L		1.050/26,67
C	.245/6,22	.255/6,48			
D	.720/18,28	.730/18,54			
E	.125/3,18				
F	.970/24,64	.980/24,89			
G	.495/12,57	.505/12,83			
H	.003/0,08	.007/0,18			
I	.090/2,29	.110/2,79			
J	.160/4,06	.175/4,45			

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